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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,113	04/14/2004	Peter J. Geiss	BUR920030152US1	3112

29154 7590 10/05/2004

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,113	GEISS ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *15-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-8 and 11-14* is/are rejected.

7)☒ Claim(s) *2,3,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-14 in the response filed 17 September 2004 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 4-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Kato. As to claim 1, Kato, Figure 11, discloses (col. 6, lines 40-60) a bipolar device comprising a base (4) and (5), an emitter (6) and (16) above said base, wherein said emitter has a T-shape with a lower section and an upper section that is wider than said lower section, spacers (13) adjacent said lower section of said emitter and beneath said upper section of said emitter, and a silicide layer (12')(col. 10, lines 30-31) adjacent said spacers and beneath said upper section of said emitter.

As to claim 4, Kato discloses (col. 7, lines 20-25) that the spacers (13) separate said emitter (16) from said silicide (12').

As to claim 5, Kato discloses that the base comprises an intrinsic base (4), and an extrinsic base (5) above said intrinsic base.

As to claim 6, Kato discloses (col. 7, lines 20-25) that the spacers (13) are insulators.

As to claim 7, Kato discloses (col. 6, lines 51-53) that layer (12), which is embodied in Figure 11 as silicide layer (12'), is formed in a self-aligned manner.

Claims 8 and 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kato. As to claim 8, Kato, Figure 11, discloses (col. 6, lines 40-60) a transistor device comprising a lower

semiconductor structure (2)(col. 6, lines 31-33) having a n-type impurity, a middle semiconductor region (4) and (5) above said lower semiconductor structure, said middle semiconductor region having a p-type impurity, an upper semiconductor structure (6) and (16) above said middle semiconductor region, wherein said upper semiconductor structure has a T-shape with a lower section and an upper section that is wider than said lower section, spacers (13) adjacent said lower section of said upper semiconductor structure and beneath said upper section of said upper semiconductor structure, and a silicide layer (12') adjacent said spacers and beneath said upper section of said upper semiconductor structure.

As to claim 11, Kato discloses (col. 7, lines 20-25) that the spacers (13) separate said upper semiconductor structure from said silicide (12').

As to claim 12, Kato discloses that the middle semiconductor region comprises an intrinsic middle semiconductor region (4), and an extrinsic middle semiconductor region (5) above said intrinsic middle semiconductor region.

As to claim 13, Kato discloses (col. 7, lines 20-25) that the spacers (13) are insulators.

As to claim 14, Kato discloses (col. 6, lines 51-53) that layer (12), which is embodied in Figure 11 as silicide layer (12'), is formed in a self-aligned manner.

Allowable Subject Matter

Claims 2, 3, 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention with a dielectric layer over the base and beneath the spacers with width less than the width of the base.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
September 29, 2004

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800